

## DIGITAL TV TUNER IC

Check for Samples: [SN761645](#)

### FEATURES

- Integrated Mixer/Oscillator/PLL and IF GCA
- VHF-L, VHF-H, UHF 3-Band Local Oscillator
- RF AGC Detector Circuit
- I2C Bus Protocol
- Seven-Step Charge Pump Current
- Four NPN Emitter-Follower Type Band Switch Drivers
- One Auxiliary Port/5-Level ADC
- Programmable Reference Divider Ratio
- Crystal Oscillator 4-MHz/16-MHz Support
- Selectable Digital IFOUT and Analog IFOUT
- Standby Mode
- 5-V Power Supply
- 38-Pin TSSOP Package

### APPLICATIONS

- Digital TV
- Digital CATV
- Set-Top Box

### DESCRIPTION

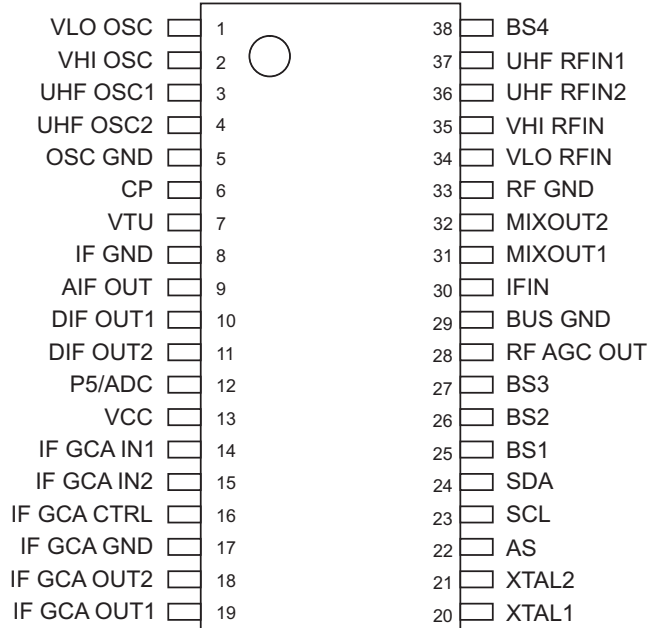
The SN761645 is a low-phase-noise synthesized tuner IC designed for digital TV tuning systems. The circuit consists of a PLL synthesizer, three-band local oscillator and mixer, RF AGC detector circuit, and IF gain controlled amplifier, and is available in a small outline package.

### ORDERING INFORMATION

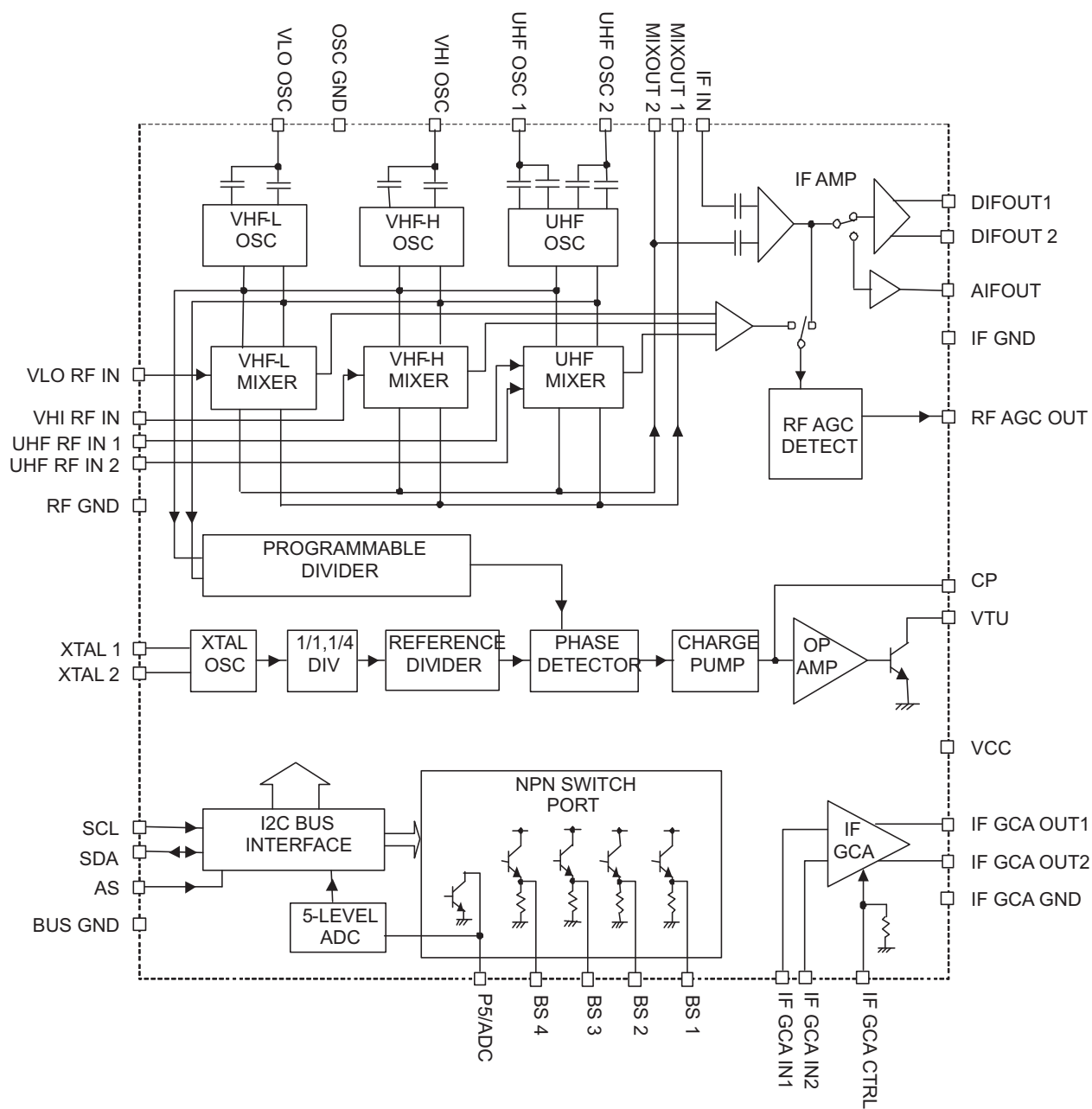
For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

DBT PACKAGE  
(TOP VIEW)

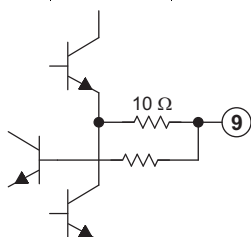
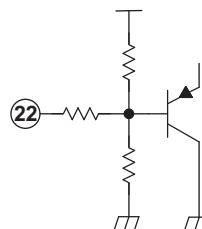


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTIONAL BLOCK DIAGRAM**

**TERMINAL FUNCTIONS**

| TERMINAL    |     | DESCRIPTION                                         | SCHEMATIC                 |
|-------------|-----|-----------------------------------------------------|---------------------------|
| NAME        | NO. |                                                     |                           |
| AIF OUT     | 9   | IF amplifier output (unbalanced)                    | <a href="#">Figure 1</a>  |
| AS          | 22  | Address selection input (open or connection to GND) | <a href="#">Figure 2</a>  |
| BS1         | 25  | Band-switch 1 output (emitter follower)             | <a href="#">Figure 3</a>  |
| BS2         | 26  | Band-switch 2 output (emitter follower)             | <a href="#">Figure 3</a>  |
| BS3         | 27  | Band-switch 3 output (emitter follower)             | <a href="#">Figure 3</a>  |
| BS4         | 38  | Band-switch 4 output (emitter follower)             | <a href="#">Figure 3</a>  |
| BUS GND     | 29  | BUS ground                                          |                           |
| CP          | 6   | Charge pump output                                  | <a href="#">Figure 4</a>  |
| DIF OUT1    | 10  | IF amplifier balance output 1                       | <a href="#">Figure 5</a>  |
| DIF OUT2    | 11  | IF amplifier balance output 2                       | <a href="#">Figure 5</a>  |
| IF GCA CTRL | 16  | IF GCA control voltage input                        | <a href="#">Figure 6</a>  |
| IF GCA GND  | 17  | IF GCA ground                                       |                           |
| IF GCA IN1  | 14  | IF GCA input 1                                      | <a href="#">Figure 7</a>  |
| IF GCA IN2  | 15  | IF GCA input 2                                      | <a href="#">Figure 7</a>  |
| IF GCA OUT1 | 19  | IF GCA output 1                                     | <a href="#">Figure 8</a>  |
| IF GCA OUT2 | 18  | IF GCA output 2                                     | <a href="#">Figure 8</a>  |
| IF GND      | 8   | IF ground                                           |                           |
| IF IN       | 30  | IF amplifier input                                  | <a href="#">Figure 9</a>  |
| MIX OUT1    | 31  | Mixer output 1                                      | <a href="#">Figure 10</a> |
| MIX OUT2    | 32  | Mixer output 2                                      | <a href="#">Figure 10</a> |
| OSC GND     | 5   | Oscillator ground                                   |                           |
| P5/ADC      | 12  | Port-5 output/ADC input                             | <a href="#">Figure 11</a> |
| RF AGC OUT  | 28  | RF AGC output                                       | <a href="#">Figure 12</a> |
| RF GND      | 33  | RF ground                                           |                           |
| SCL         | 23  | Serial clock input                                  | <a href="#">Figure 13</a> |
| SDA         | 24  | Serial data input/output                            | <a href="#">Figure 14</a> |
| UHF OSC1    | 3   | UHF oscillator 1                                    | <a href="#">Figure 15</a> |
| UHF OSC2    | 4   | UHF oscillator 2                                    | <a href="#">Figure 15</a> |
| UHF RF IN1  | 37  | UHF RF input 1                                      | <a href="#">Figure 16</a> |
| UHF RF IN2  | 36  | UHF RF input 2                                      | <a href="#">Figure 16</a> |
| VCC         | 13  | Supply voltage                                      |                           |
| VHI OSC     | 2   | VHF HIGH oscillator                                 | <a href="#">Figure 17</a> |
| VHI RF IN   | 35  | VHF HIGH RF input                                   | <a href="#">Figure 18</a> |
| VLO OSC     | 1   | VHF LOW oscillator                                  | <a href="#">Figure 19</a> |
| VLO RF IN   | 34  | VHF LOW RF input                                    | <a href="#">Figure 20</a> |
| VTU         | 7   | Tuning voltage amplifier output                     | <a href="#">Figure 21</a> |
| XTAL1       | 20  | Crystal oscillator                                  | <a href="#">Figure 22</a> |
| XTAL2       | 21  | Crystal oscillator                                  | <a href="#">Figure 22</a> |


**Figure 1. AIF OUT**

**Figure 2. AS**

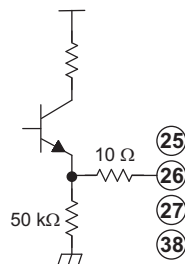


Figure 3. BS1, BS2, BS3, BS4

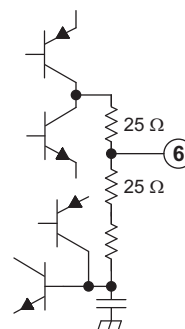


Figure 4. CP

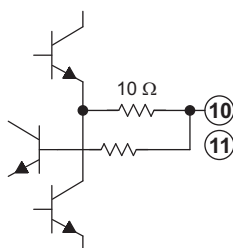


Figure 5. DIF OUT1, DIF OUT2

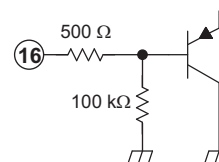


Figure 6. IF GCA CTRL

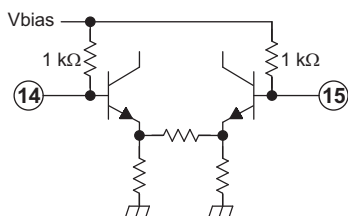


Figure 7. IF GCA IN1, IF GCA IN2

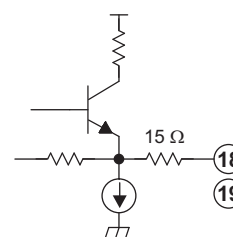


Figure 8. IF GCA OUT1, IF GCA OUT2

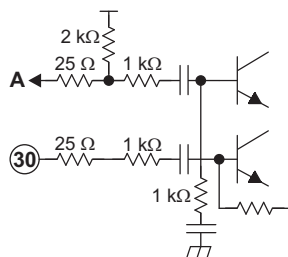


Figure 9. IF IN

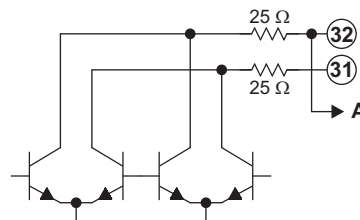


Figure 10. MIXOUT1, MIXOUT2

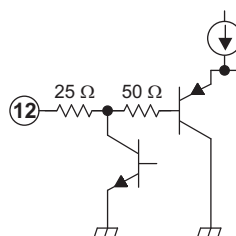


Figure 11. P5/ADC

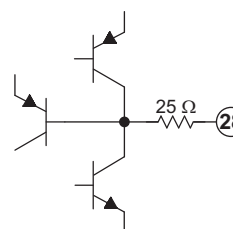


Figure 12. RF AGC OUT

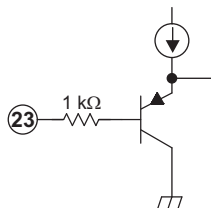


**Figure 13. SCL**

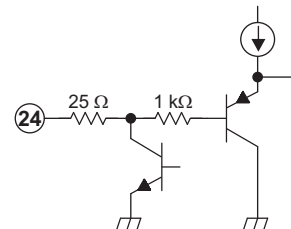


**Figure 14. SDA**

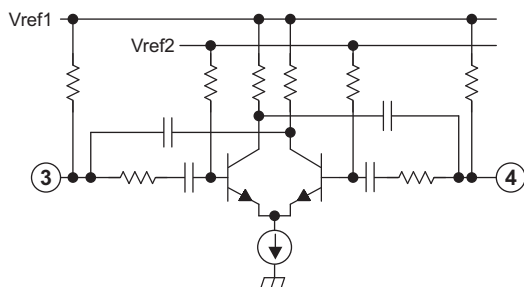


**Figure 15. UHF OSC 1, UHF OSC 2**

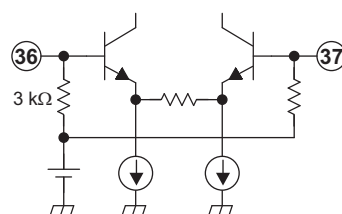


**Figure 16. UHF RF IN1, UHF RF IN2**

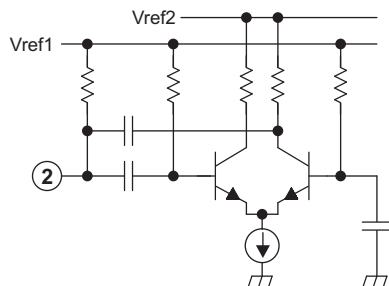


**Figure 17. VHI OSC**

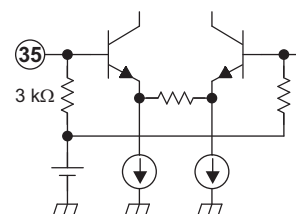


**Figure 18. VHI RF IN**

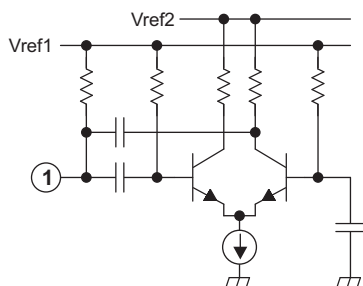


**Figure 19. VLO OSC**

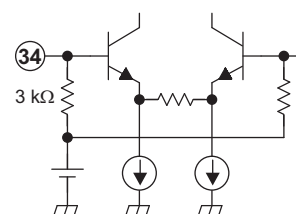


**Figure 20. VLO RF IN**

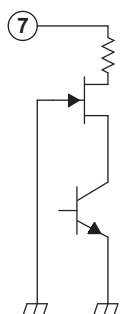


**Figure 21. VTU**

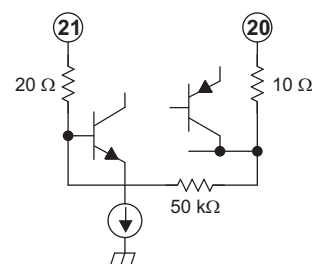


**Figure 22. XTAL1, XTAL2**

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

|                      |                                             |                                       | MIN  | MAX  | UNIT |
|----------------------|---------------------------------------------|---------------------------------------|------|------|------|
| V <sub>CC</sub>      | Supply voltage range <sup>(2)</sup>         | V <sub>CC</sub>                       | –0.4 | 6.5  | V    |
| V <sub>GND</sub>     | Input voltage range 1 <sup>(2)</sup>        | RF GND, OSC GND, BUS GND              | –0.4 | 0.4  | V    |
| VTU                  | Input voltage range 2 <sup>(2)</sup>        | VTU                                   | –0.4 | 35   | V    |
| V <sub>IN</sub>      | Input voltage range 3 <sup>(2)</sup>        | Other pins                            | –0.4 | 6.5  | V    |
| P <sub>D</sub>       | Continuous total dissipation <sup>(3)</sup> | T <sub>A</sub> ≤ 25°C                 |      | 1277 | mW   |
| T <sub>A</sub>       | Operating free-air temperature range        |                                       | –20  | 85   | °C   |
| T <sub>stg</sub>     | Storage temperature range                   |                                       | –65  | 150  | °C   |
| T <sub>J</sub>       | Maximum junction temperature                |                                       |      | 150  | °C   |
| t <sub>SC(max)</sub> | Maximum short-circuit time                  | Each pin to V <sub>CC</sub> or to GND |      | 10   | s    |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage values are with respect to the IF GND of the circuit.
- (3) Derating factor is 10.2 mW/°C for T<sub>A</sub> > 25°C.

## RECOMMENDED OPERATING CONDITIONS

|                 |                                |                                | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|--------------------------------|-----|-----|-----|------|
| V <sub>CC</sub> | Supply voltage                 | V <sub>CC</sub>                | 4.5 | 5   | 5.3 | V    |
| VTU             | Tuning supply voltage          | VTU                            |     | 30  | 33  | V    |
| I <sub>BS</sub> | Output current of band switch  | BS1 to BS4, one band switch on |     |     | 10  | mA   |
| I <sub>P5</sub> | Output current of port 5       | P5                             |     |     | –5  | mA   |
| T <sub>A</sub>  | Operating free-air temperature |                                | –20 |     | 85  | °C   |



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

IF IN1, MIX OUT 1, and MIX OUT 2 (pins 30, 31, and 32, respectively) withstand 1.5 kV, and all other pins withstand 2 kV, according to the Human-Body Model (1.5 kΩ, 100 pF).

## ELECTRICAL CHARACTERISTICS

### Total Device and Serial Interface

 $V_{CC} = 4.5\text{ V to }5.3\text{ V}$ ,  $T_A = -20^{\circ}\text{C to }85^{\circ}\text{C}$  (unless otherwise noted)

| PARAMETER                       |                                                                                              | TEST CONDITIONS                                | MIN | TYP | MAX      | UNIT          |
|---------------------------------|----------------------------------------------------------------------------------------------|------------------------------------------------|-----|-----|----------|---------------|
| $I_{CC1}$                       | Supply current 1                                                                             | BS[1:4] = 0100, IFGCA disabled                 |     | 90  |          | mA            |
| $I_{CC2}$                       | Supply current 2                                                                             | BS[1:4] = 0100, IFGCA enabled                  |     | 110 |          | mA            |
| $I_{CC-STBY}$                   | Standby supply current                                                                       | BS[1:4] = 1100                                 |     | 9   |          | mA            |
| $V_{IH}$                        | High-level input voltage (SCL, SDA)                                                          |                                                | 2.3 |     |          | V             |
| $V_{IL}$                        | Low-level input voltage (SCL, SDA)                                                           |                                                |     |     | 1.05     | V             |
| $I_{IH}$                        | High-level input current (SCL, SDA)                                                          |                                                |     |     | 10       | $\mu\text{A}$ |
| $I_{IL}$                        | Low-level input current (SCL, SDA)                                                           |                                                | -10 |     |          | $\mu\text{A}$ |
| $V_{POR}$                       | Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode) |                                                | 2.1 | 2.8 | 3.5      | V             |
| <b>I<sup>2</sup>C Interface</b> |                                                                                              |                                                |     |     |          |               |
| $V_{ADC}$                       | ADC input voltage                                                                            | See <a href="#">Table 11</a>                   | 0   |     | $V_{CC}$ | V             |
| $I_{ADH}$                       | ADC high-level input current                                                                 | $V_{ADC} = V_{CC}$                             |     |     | 10       | $\mu\text{A}$ |
| $I_{ADL}$                       | ADC low-level input current                                                                  | $V_{ADC} = 0\text{ V}$                         | -10 |     |          | $\mu\text{A}$ |
| $V_{OL}$                        | Low-level output voltage (SDA)                                                               | $V_{CC} = 5\text{ V}$ , $I_{OL} = 3\text{ mA}$ |     |     | 0.4      | V             |
| $I_{SDAH}$                      | High-level output leakage current (SDA)                                                      | $V_{SDA} = 5.3\text{ V}$                       |     |     | 10       | $\mu\text{A}$ |
| $f_{SCL}$                       | Clock frequency (SCL)                                                                        |                                                |     | 100 | 400      | kHz           |
| $t_{HD-DAT}$                    | Data hold time                                                                               | See <a href="#">Figure 23</a>                  | 0   |     | 3.45     | $\mu\text{s}$ |
| $t_{BUF}$                       | Bus free time                                                                                |                                                | 1.3 |     |          | $\mu\text{s}$ |
| $t_{HD-STA}$                    | Start hold time                                                                              |                                                | 0.6 |     |          | $\mu\text{s}$ |
| $t_{LOW}$                       | SCL-low hold time                                                                            |                                                | 1.3 |     |          | $\mu\text{s}$ |
| $t_{HIGH}$                      | SCL-high hold time                                                                           |                                                | 0.6 |     |          | $\mu\text{s}$ |
| $t_{SU-STA}$                    | Start setup time                                                                             |                                                | 0.6 |     |          | $\mu\text{s}$ |
| $t_{SU-DAT}$                    | Data setup time                                                                              |                                                | 0.1 |     |          | $\mu\text{s}$ |
| $t_r$                           | Rise time (SCL, SDA )                                                                        |                                                |     |     | 1        | $\mu\text{s}$ |
| $t_f$                           | Fall time (SCL, SDA)                                                                         |                                                |     |     | 0.3      | $\mu\text{s}$ |
| $t_{SU-STO}$                    | Stop setup time                                                                              |                                                | 0.6 |     |          | $\mu\text{s}$ |

## PLL and Band Switch

$V_{CC} = 4.5\text{ V to }5.3\text{ V}$ ,  $T_A = -20^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER    |                                              | TEST CONDITIONS                                                            | MIN | TYP  | MAX   | UNIT          |
|--------------|----------------------------------------------|----------------------------------------------------------------------------|-----|------|-------|---------------|
| N            | Divider ratio                                | 15-bit frequency word                                                      | 512 |      | 32767 |               |
| $f_{XTAL}$   | Crystal oscillator frequency                 | $R_{XTAL} = 25\ \Omega$ to $300\ \Omega$                                   |     | 4    | 16    | MHz           |
| $Z_{XTAL}$   | Crystal oscillator input impedance           | 4-MHz crystal, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$            |     | 2    |       | k $\Omega$    |
| $V_{VTUL}$   | Tuning amplifier low-level output voltage    | $R_L = 20\text{ k}\Omega$ , $VTU = 33\text{ V}$                            | 0.2 | 0.45 | 0.6   | V             |
| $I_{VTUOFF}$ | Tuning amplifier leakage current             | Tuning amplifier = off, $VTU = 33\text{ V}$                                |     |      | 10    | $\mu\text{A}$ |
| $I_{CP000}$  | Charge-pump current                          | CP[2:0] = 000                                                              |     | 35   |       | $\mu\text{A}$ |
| $I_{CP001}$  |                                              | CP[2:0] = 001                                                              |     | 70   |       |               |
| $I_{CP010}$  |                                              | CP[2:0] = 010                                                              |     | 140  |       |               |
| $I_{CP011}$  |                                              | CP[2:0] = 011                                                              |     | 210  |       |               |
| $I_{CP100}$  |                                              | CP[2:0] = 100                                                              |     | 280  |       |               |
| $I_{CP101}$  |                                              | CP[2:0] = 101                                                              |     | 350  |       |               |
| $I_{CP110}$  |                                              | CP[2:0] = 110                                                              |     | 420  |       |               |
| $V_{CP}$     | Charge-pump output voltage                   | PLL locked                                                                 |     | 1.95 |       | V             |
| $I_{CPOFF}$  | Charge-pump leakage current                  | $V_{CP} = 2\text{ V}$ , $T_A = 25^\circ\text{C}$                           | -15 |      | 15    | nA            |
| $I_{BS}$     | Band switch driver output current (BS1–BS4)  |                                                                            |     |      | 10    | mA            |
| $V_{BS1}$    | Band switch driver output voltage (BS1–BS4)  | $I_{BS} = 10\text{ mA}$                                                    |     | 2.9  |       | V             |
| $V_{BS2}$    |                                              | $I_{BS} = 10\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ | 3.4 | 3.6  |       |               |
| $I_{BSOFF}$  | Band switch driver leakage current (BS1–BS4) | $V_{BS} = 0\text{ V}$                                                      |     |      | 8     | $\mu\text{A}$ |
| $I_{P5}$     | Band switch port sink current (P5/ADC)       |                                                                            | -5  |      |       | mA            |
| $V_{P5ON}$   | Band switch port output voltage (P5/ADC)     | $I_{P5} = -2\text{ mA}$ , $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ |     |      | 0.6   | V             |

## RF AGC<sup>(1)</sup>

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , measured in Figure 24 reference measurement circuit at 50- $\Omega$  system, IF = 36.15 MHz (unless otherwise noted)

| PARAMETER      |                                          | TEST CONDITIONS | MIN            | TYP | MAX | UNIT             |
|----------------|------------------------------------------|-----------------|----------------|-----|-----|------------------|
| $I_{OAGC0}$    | RF AGC output source current             | ATC = 0         |                | 300 |     | nA               |
| $I_{OAGC1}$    |                                          | ATC = 1         |                | 9   |     | $\mu\text{A}$    |
| $I_{OAGCSINK}$ | RF AGC peak sink current                 | ATC = 0         |                | 100 |     | $\mu\text{A}$    |
| $V_{OAGCH}$    | RFAGCOUT output high voltage (max level) | ATC = 1         | 3.7            | 4.2 | 4.7 | V                |
| $V_{OAGCL}$    | RFAGCOUT output low voltage (min level)  | ATC = 1         |                | 0.3 |     | V                |
| $V_{AGCSP00}$  | Start-point IF output level              | AISL = 0        | ATP[2:0] = 000 |     | 114 | dB $\mu\text{V}$ |
| $V_{AGCSP01}$  |                                          |                 | ATP[2:0] = 001 |     | 112 |                  |
| $V_{AGCSP02}$  |                                          |                 | ATP[2:0] = 010 |     | 110 |                  |
| $V_{AGCSP03}$  |                                          |                 | ATP[2:0] = 011 |     | 108 |                  |
| $V_{AGCSP04}$  |                                          |                 | ATP[2:0] = 100 |     | 106 |                  |
| $V_{AGCSP05}$  |                                          |                 | ATP[2:0] = 101 |     | 104 |                  |
| $V_{AGCSP06}$  |                                          |                 | ATP[2:0] = 110 |     | 102 |                  |

(1) When AISL = 1, RF AGC function is not available at VHF-L band.

## Mixer, Oscillator, IF Amplifier (DIF OUT)

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , measured in [Figure 24](#) reference measurement circuit at 50- $\Omega$  system, IF = 36.15 MHz (unless otherwise noted)

| PARAMETER          |                                                                | TEST CONDITIONS                    | MIN | TYP | MAX | UNIT             |
|--------------------|----------------------------------------------------------------|------------------------------------|-----|-----|-----|------------------|
| GC <sub>1D</sub>   | Conversion gain (mixer - IF amplifier), VHF-LOW                | $f_{IN} = 50.85\text{ MHz}^{(1)}$  |     | 35  |     | dB               |
| GC <sub>3D</sub>   |                                                                | $f_{IN} = 149.85\text{ MHz}^{(1)}$ |     | 35  |     | dB               |
| GC <sub>4D</sub>   | Conversion gain (mixer - IF amplifier), VHF-HIGH               | $f_{IN} = 156.85\text{ MHz}^{(1)}$ |     | 35  |     | dB               |
| GC <sub>6D</sub>   |                                                                | $f_{IN} = 425.85\text{ MHz}^{(1)}$ |     | 35  |     | dB               |
| GC <sub>7D</sub>   | Conversion gain (mixer - IF amplifier), UHF                    | $f_{IN} = 433.85\text{ MHz}^{(1)}$ |     | 35  |     | dB               |
| GC <sub>9D</sub>   |                                                                | $f_{IN} = 857.85\text{ MHz}^{(1)}$ |     | 35  |     | dB               |
| NF <sub>1D</sub>   | Noise figure, VHF-LOW                                          | $f_{IN} = 50.85\text{ MHz}$        |     | 9   |     | dB               |
| NF <sub>3D</sub>   |                                                                | $f_{IN} = 149.85\text{ MHz}$       |     | 9   |     | dB               |
| NF <sub>4D</sub>   | Noise figure, VHF-HIGH                                         | $f_{IN} = 156.85\text{ MHz}$       |     | 9   |     | dB               |
| NF <sub>6D</sub>   |                                                                | $f_{IN} = 425.85\text{ MHz}$       |     | 10  |     | dB               |
| NF <sub>7D</sub>   | Noise figure, UHF                                              | $f_{IN} = 433.85\text{ MHz}$       |     | 10  |     | dB               |
| NF <sub>9D</sub>   |                                                                | $f_{IN} = 857.85\text{ MHz}$       |     | 11  |     | dB               |
| CM <sub>1D</sub>   | Input voltage causing 1% cross modulation distortion, VHF-LOW  | $f_{IN} = 50.85\text{ MHz}^{(2)}$  |     | 92  |     | dB $\mu\text{V}$ |
| CM <sub>3D</sub>   |                                                                | $f_{IN} = 149.85\text{ MHz}^{(2)}$ |     | 92  |     | dB $\mu\text{V}$ |
| CM <sub>4D</sub>   | Input voltage causing 1% cross modulation distortion, VHF-HIGH | $f_{IN} = 156.85\text{ MHz}^{(2)}$ |     | 92  |     | dB $\mu\text{V}$ |
| CM <sub>6D</sub>   |                                                                | $f_{IN} = 425.85\text{ MHz}^{(2)}$ |     | 92  |     | dB $\mu\text{V}$ |
| CM <sub>7D</sub>   | Input voltage causing 1% cross modulation distortion, UHF      | $f_{IN} = 433.85\text{ MHz}^{(2)}$ |     | 92  |     | dB $\mu\text{V}$ |
| CM <sub>9D</sub>   |                                                                | $f_{IN} = 857.85\text{ MHz}^{(2)}$ |     | 92  |     | dB $\mu\text{V}$ |
| V <sub>IFO1D</sub> | IF output voltage, VHF-LOW                                     | $f_{IN} = 50.85\text{ MHz}$        |     | 117 |     | dB $\mu\text{V}$ |
| V <sub>IFO3D</sub> |                                                                | $f_{IN} = 149.85\text{ MHz}$       |     | 117 |     | dB $\mu\text{V}$ |
| V <sub>IFO4D</sub> | IF output voltage, VHF-HIGH                                    | $f_{IN} = 156.85\text{ MHz}$       |     | 117 |     | dB $\mu\text{V}$ |
| V <sub>IFO6D</sub> |                                                                | $f_{IN} = 425.85\text{ MHz}$       |     | 117 |     | dB $\mu\text{V}$ |
| V <sub>IFO7D</sub> | IF output voltage, UHF                                         | $f_{IN} = 433.85\text{ MHz}$       |     | 117 |     | dB $\mu\text{V}$ |
| V <sub>IFO9D</sub> |                                                                | $f_{IN} = 857.85\text{ MHz}$       |     | 117 |     | dB $\mu\text{V}$ |
| $\Phi_{PLVL1D}$    | Phase noise, VHF-LOW                                           | $f_{IN} = 50.85\text{ MHz}^{(3)}$  |     | -92 |     | dBc/Hz           |
| $\Phi_{PLVL3D}$    |                                                                | $f_{IN} = 149.85\text{ MHz}^{(4)}$ |     | -91 |     | dBc/Hz           |
| $\Phi_{PLVL4D}$    | Phase noise, VHF-HIGH                                          | $f_{IN} = 156.85\text{ MHz}^{(3)}$ |     | -86 |     | dBc/Hz           |
| $\Phi_{PLVL6D}$    |                                                                | $f_{IN} = 425.85\text{ MHz}^{(4)}$ |     | -83 |     | dBc/Hz           |
| $\Phi_{PLVL7D}$    | Phase noise, UHF                                               | $f_{IN} = 433.85\text{ MHz}^{(3)}$ |     | -79 |     | dBc/Hz           |
| $\Phi_{PLVL9D}$    |                                                                | $f_{IN} = 857.85\text{ MHz}^{(4)}$ |     | -77 |     | dBc/Hz           |

(1) RF input level = 70 dB $\mu\text{V}$ , differential output

(2)  $f_{undes} = f_{des} \pm 7\text{ MHz}$ , Pin = 70 dB $\mu\text{V}$ , AM 1 kHz, 30%, DES/CM = S/I = 46 dB

(3) Offset = 1 kHz, CP current = 70  $\mu\text{A}$ , reference divider = 24

(4) Offset = 1 kHz, CP current = 420  $\mu\text{A}$ , reference divider = 24

## Mixer, Oscillator, IF Amplifier (AIF OUT)

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , measured in [Figure 24](#) reference measurement circuit at 50- $\Omega$  system, IF = 36.15 MHz (unless otherwise noted)

| PARAMETER          |                                                                | TEST CONDITIONS                    | MIN | TYP | MAX | UNIT       |
|--------------------|----------------------------------------------------------------|------------------------------------|-----|-----|-----|------------|
| GC <sub>1A</sub>   | Conversion gain (mixer - IF amplifier), VHF-LOW                | $f_{IN} = 50.85\text{ MHz}^{(1)}$  |     | 29  |     | dB         |
| GC <sub>3A</sub>   |                                                                | $f_{IN} = 149.85\text{ MHz}^{(1)}$ |     | 29  |     | dB         |
| GC <sub>4A</sub>   | Conversion gain (mixer - IF amplifier), VHF-HIGH               | $f_{IN} = 156.85\text{ MHz}^{(1)}$ |     | 29  |     | dB         |
| GC <sub>6A</sub>   |                                                                | $f_{IN} = 425.85\text{ MHz}^{(1)}$ |     | 29  |     | dB         |
| GC <sub>7A</sub>   | Conversion gain (mixer - IF amplifier), UHF                    | $f_{IN} = 433.85\text{ MHz}^{(1)}$ |     | 29  |     | dB         |
| GC <sub>9A</sub>   |                                                                | $f_{IN} = 857.85\text{ MHz}^{(1)}$ |     | 29  |     | dB         |
| NF <sub>1A</sub>   | Noise figure, VHF-LOW                                          | $f_{IN} = 50.85\text{ MHz}$        |     | 9   |     | dB         |
| NF <sub>3A</sub>   |                                                                | $f_{IN} = 149.85\text{ MHz}$       |     | 9   |     | dB         |
| NF <sub>4A</sub>   | Noise figure, VHF-HIGH                                         | $f_{IN} = 156.85\text{ MHz}$       |     | 9   |     | dB         |
| NF <sub>6A</sub>   |                                                                | $f_{IN} = 425.85\text{ MHz}$       |     | 10  |     | dB         |
| NF <sub>7A</sub>   | Noise figure, UHF                                              | $f_{IN} = 433.85\text{ MHz}$       |     | 10  |     | dB         |
| NF <sub>9A</sub>   |                                                                | $f_{IN} = 857.85\text{ MHz}$       |     | 11  |     | dB         |
| CM <sub>1A</sub>   | Input voltage causing 1% cross modulation distortion, VHF-LOW  | $f_{IN} = 50.85\text{ MHz}^{(2)}$  |     | 87  |     | dB $\mu$ V |
| CM <sub>3A</sub>   |                                                                | $f_{IN} = 149.85\text{ MHz}^{(2)}$ |     | 87  |     | dB $\mu$ V |
| CM <sub>4A</sub>   | Input voltage causing 1% cross modulation distortion, VHF-HIGH | $f_{IN} = 156.85\text{ MHz}^{(2)}$ |     | 87  |     | dB $\mu$ V |
| CM <sub>6A</sub>   |                                                                | $f_{IN} = 425.85\text{ MHz}^{(2)}$ |     | 87  |     | dB $\mu$ V |
| CM <sub>7A</sub>   | Input voltage causing 1% cross modulation distortion, UHF      | $f_{IN} = 433.85\text{ MHz}^{(2)}$ |     | 87  |     | dB $\mu$ V |
| CM <sub>9A</sub>   |                                                                | $f_{IN} = 857.85\text{ MHz}^{(2)}$ |     | 87  |     | dB $\mu$ V |
| V <sub>IF01A</sub> | IF output voltage, VHF-LOW                                     | $f_{IN} = 50.85\text{ MHz}$        |     | 117 |     | dB $\mu$ V |
| V <sub>IF03A</sub> |                                                                | $f_{IN} = 149.85\text{ MHz}$       |     | 117 |     | dB $\mu$ V |
| V <sub>IF04A</sub> | IF output voltage, VHF-HIGH                                    | $f_{IN} = 156.85\text{ MHz}$       |     | 117 |     | dB $\mu$ V |
| V <sub>IF06A</sub> |                                                                | $f_{IN} = 425.85\text{ MHz}$       |     | 117 |     | dB $\mu$ V |
| V <sub>IF07A</sub> | IF output voltage, UHF                                         | $f_{IN} = 433.85\text{ MHz}$       |     | 117 |     | dB $\mu$ V |
| V <sub>IF09A</sub> |                                                                | $f_{IN} = 857.85\text{ MHz}$       |     | 117 |     | dB $\mu$ V |
| $\Phi_{PLVL1A}$    | Phase noise, VHF-LOW                                           | $f_{IN} = 50.85\text{ MHz}^{(3)}$  |     | -92 |     | dBc/Hz     |
| $\Phi_{PLVL3A}$    |                                                                | $f_{IN} = 149.85\text{ MHz}^{(3)}$ |     | -96 |     | dBc/Hz     |
| $\Phi_{PLVL4A}$    | Phase noise, VHF-HIGH                                          | $f_{IN} = 156.85\text{ MHz}^{(3)}$ |     | -85 |     | dBc/Hz     |
| $\Phi_{PLVL6A}$    |                                                                | $f_{IN} = 425.85\text{ MHz}^{(3)}$ |     | -88 |     | dBc/Hz     |
| $\Phi_{PLVL7A}$    | Phase noise, UHF                                               | $f_{IN} = 433.85\text{ MHz}^{(3)}$ |     | -80 |     | dBc/Hz     |
| $\Phi_{PLVL9A}$    |                                                                | $f_{IN} = 857.85\text{ MHz}^{(3)}$ |     | -85 |     | dBc/Hz     |

(1) RF input level = 70 dB $\mu$ V

(2)  $f_{undes} = f_{des} \pm 7\text{ MHz}$ , Pin = 70 dB $\mu$ V, AM 1 kHz, 30%, DES/CM = S/I = 46 dB

(3) Offset = 10 kHz, CP current = 35  $\mu$ A, reference divider = 64

## IF Gain Controlled Amplifier

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , measured in [Figure 24](#) reference measurement circuit at 50- $\Omega$  system,  $f_{IF} = f_{IF} = 36.15\text{ MHz}$  (unless otherwise noted)

| PARAMETER      |                                              | TEST CONDITIONS                                                                                                                            | MIN | TYP | MAX      | UNIT            |
|----------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|----------|-----------------|
| $I_{IFGCA}$    | Input current (IF GCA CTRL)                  | $V_{IFGCA} = 3\text{ V}$                                                                                                                   |     | 60  | 90       | $\mu\text{A}$   |
| $V_{IFGCAMAX}$ | Maximum gain control voltage                 | Gain maximum                                                                                                                               | 3   |     | $V_{CC}$ | V               |
| $V_{IFGCAMIN}$ | Minimum gain control voltage                 | Gain minimum                                                                                                                               | 0   |     | 0.2      | V               |
| $G_{IFGCAMAX}$ | Maximum gain                                 | $V_{IFGCA} = 3\text{ V}$                                                                                                                   |     | 67  |          | dB              |
| $G_{IFGCAMIN}$ | Minimum gain                                 | $V_{IFGCA} = 0\text{ V}$                                                                                                                   |     | 3   |          | dB              |
| $GCR_{IFGCA}$  | Gain control range                           | $V_{IFGCA} = 0\text{ V to } 3\text{ V}$                                                                                                    |     | 64  |          | dB              |
| $V_{IFGCAOUT}$ | Output voltage                               | Single-ended output,<br>$V_{IFGCA} = 3\text{ V}$                                                                                           |     | 2.1 |          | V <sub>pp</sub> |
| $NF_{IFGCA}$   | Noise figure                                 | $V_{IFGCA} = 3\text{ V}$                                                                                                                   |     | 11  |          | dB              |
| $IM3_{IFGCA}$  | Third order intermodulation distortion       | $f_{IFGCAIN1} = 35.65\text{ MHz}$ ,<br>$f_{IFGCAIN2} = 36.65\text{ MHz}$ ,<br>$V_{IFGCAOUT} = -2\text{ dBm}$ ,<br>$V_{IFGCA} = 3\text{ V}$ |     | -50 |          | dBc             |
| $IIP_{3IFGCA}$ | Input intercept point                        | $V_{IFGCA} = 0\text{ V}$                                                                                                                   |     | 11  |          | dBm             |
| $R_{IFGCAIN}$  | Input resistance (IF GCA IN1, IF GCA IN2)    |                                                                                                                                            |     | 1   |          | k $\Omega$      |
| $R_{IFGCAOUT}$ | Output resistance (IF GCA OUT1, IF GCA OUT2) |                                                                                                                                            |     | 25  |          | $\Omega$        |

## FUNCTIONAL DESCRIPTION

### I<sup>2</sup>C Bus Mode

#### I<sup>2</sup>C Write Mode ( $R/\overline{W} = 0$ )

**Table 1. Write Data Format**

|                       | MSB |     |      |      |        |      |     | LSB     |                  |
|-----------------------|-----|-----|------|------|--------|------|-----|---------|------------------|
| Address Byte (ADB)    | 1   | 1   | 0    | 0    | 0      | 0    | MA  | R/W = 0 | A <sup>(1)</sup> |
| Divider Byte 1 (DB1)  | 0   | N14 | N13  | N12  | N11    | N10  | N9  | N8      | A <sup>(1)</sup> |
| Divider Byte 2 (DB2)  | N7  | N6  | N5   | N4   | N3     | N2   | N1  | N0      | A <sup>(1)</sup> |
| Control Byte 1 (CB1)  | 1   | 0   | ATP2 | ATP1 | ATP0   | RS2  | RS1 | RS0     | A <sup>(1)</sup> |
| Band Switch Byte (BB) | CP1 | CP0 | AISL | P5   | BS4    | BS3  | BS2 | BS1     | A <sup>(1)</sup> |
| Control Byte 2 (CB2)  | 1   | 1   | ATC  | MODE | DISGCA | IFDA | CP2 | IXD4    | A <sup>(1)</sup> |

(1) A = acknowledge

**Table 2. Write Data Symbol Description**

| SYMBOL   | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                         | DEFAULT                          |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|-----|--|---|---|--------|---|---|--------|---|---|-----|---|---|----------------------------------|----------------|
| MA       | Address set bit<br>MA = 0 : AS pin = 0 V (connection to GND)<br>MA = 1 : AS pin = Open                                                                                                                                                                                                                                                                                                                                                                              |                                  |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| N[14:0]  | Programmable counter set bits<br>$N = N14 \times 2^{14} + N13 \times 2^{13} + \dots + N1 \times 2 + N0$                                                                                                                                                                                                                                                                                                                                                             | N14 = N13 = N12 = ... = N0 = 0   |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| ATP[2:0] | RF AGC start-point control bits (see Table 3)                                                                                                                                                                                                                                                                                                                                                                                                                       | ATP[2:0] = 000                   |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| RS[2:0]  | Reference divider ratio-selection bits (see Table 4)                                                                                                                                                                                                                                                                                                                                                                                                                | RS[2:0] = 000                    |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| CP[2:0]  | Charge-pump current set bits (see Table 5)                                                                                                                                                                                                                                                                                                                                                                                                                          | CP[2:0] = 000                    |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| P5       | Port output / ADC input control bit<br>P5 = 0 : ADC input<br>P5 = 1 : Tr = ON                                                                                                                                                                                                                                                                                                                                                                                       | P5 = 0                           |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| BS[4:1]  | Band-switch driver output control bits<br>BSn = 0: Tr = OFF<br>BSn = 1: Tr = ON<br><br>Band selection and standby function control bits<br><table border="1"> <thead> <tr> <th>BS2</th><th>BS1</th><th></th></tr> </thead> <tbody> <tr> <td>0</td><td>1</td><td>VHF-LO</td></tr> <tr> <td>1</td><td>0</td><td>VHF-HI</td></tr> <tr> <td>0</td><td>0</td><td>UHF</td></tr> <tr> <td>1</td><td>1</td><td>Standby mode / stop MOP function</td></tr> </tbody> </table> | BS2                              | BS1 |  | 0 | 1 | VHF-LO | 1 | 0 | VHF-HI | 0 | 0 | UHF | 1 | 1 | Standby mode / stop MOP function | BS[4:1] = 0000 |
| BS2      | BS1                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                  |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| 0        | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | VHF-LO                           |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| 1        | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | VHF-HI                           |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| 0        | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | UHF                              |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| 1        | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Standby mode / stop MOP function |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| ATC      | RFAGC output current-set bit<br>ATC = 0: Source current = 300nA<br>ATC = 1: Source current = 9uA                                                                                                                                                                                                                                                                                                                                                                    | ATC = 0                          |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| MODE     | Device mode selection bit<br>MODE = 0 : Test mode<br>MODE = 1 : Normal operation                                                                                                                                                                                                                                                                                                                                                                                    | MODE = 0                         |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| DISGCA   | Other control bits<br>DISGCA IF GCA control bit (see Table 6)                                                                                                                                                                                                                                                                                                                                                                                                       | DISGCA = 0                       |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| IFDA     | IFDA AIF/DIF OUT selection bit (see Table 7)                                                                                                                                                                                                                                                                                                                                                                                                                        | IFDA = 0                         |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| AISL     | AISL RFAGC detector input selection bit (see Table 8)                                                                                                                                                                                                                                                                                                                                                                                                               | AISL = 0                         |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |
| IXD4     | IXD4 Reference divider control bit (see Table 4)                                                                                                                                                                                                                                                                                                                                                                                                                    | IXD4 = 0                         |     |  |   |   |        |   |   |        |   |   |     |   |   |                                  |                |

**Table 3. RF AGC Start Point**

| MODE | ATP2 | ATP1 | ATP0 | IFOUT LEVEL  |         |
|------|------|------|------|--------------|---------|
|      |      |      |      | (dB $\mu$ V) | (mVp-p) |
| 1    | 0    | 0    | 0    | 114          | 1417    |
| 1    | 0    | 0    | 1    | 112          | 1126    |
| 1    | 0    | 1    | 0    | 110          | 894     |
| 1    | 0    | 1    | 1    | 108          | 710     |
| 1    | 1    | 0    | 0    | 106          | 564     |
| 1    | 1    | 0    | 1    | 104          | 448     |
| 1    | 1    | 1    | 0    | 102          | 356     |
| 1    | 1    | 1    | 1    | Disabled     |         |

**Table 4. Reference Divider Ratio**

| MODE | IXD4 | RS2 | RS1 | RS0 | REFERENCE DIVIDER RATIO |
|------|------|-----|-----|-----|-------------------------|
| 1    | 0    | 0   | 0   | 0   | 96                      |
| 1    | 0    | 0   | 0   | 1   | 112                     |
| 1    | 0    | 0   | 1   | 0   | 128                     |
| 1    | 0    | 0   | 1   | 1   | 256                     |
| 1    | 0    | 1   | 0   | 0   | 512                     |
| 1    | 0    | 1   | 0   | 1   | 320                     |
| 1    | 1    | 0   | 0   | 0   | 24                      |
| 1    | 1    | 0   | 0   | 1   | 28                      |
| 1    | 1    | 0   | 1   | 0   | 32                      |
| 1    | 1    | 0   | 1   | 1   | 64                      |
| 1    | 1    | 1   | 0   | 0   | 128                     |
| 1    | 1    | 1   | 0   | 1   | 80                      |
| 1    | X    | 1   | 1   | 1   | Forbidden               |

**Table 5. Charge-Pump Current**

| MODE | CP2 | CP1 | CP0 | CHARGE PUMP CURRENT ( $\mu$ A) |
|------|-----|-----|-----|--------------------------------|
| 1    | 0   | 0   | 0   | 35                             |
| 1    | 0   | 0   | 1   | 70                             |
| 1    | 0   | 1   | 0   | 140                            |
| 1    | 0   | 1   | 1   | 210                            |
| 1    | 1   | 0   | 0   | 280                            |
| 1    | 1   | 0   | 1   | 350                            |
| 1    | 1   | 1   | 0   | 420                            |
| 1    | 1   | 1   | 1   | Forbidden                      |

**Table 6. IF GCA Control**

| MODE | DISGCA | IF GCA FUNCTION |
|------|--------|-----------------|
| 1    | 0      | IF GCA enabled  |
| 1    | 1      | IF GCA disabled |

**Table 7. AIF / DIF OUT Selection**

| MODE | IFDA | IF OUT FUNCTION      |
|------|------|----------------------|
| 1    | 0    | DIF OUT 1,2 selected |
| 1    | 1    | AIF OUT selected     |

**Table 8. RF AGC Detector Input Selection**

| MODE | AISL             | RF AGC DETECTOR INPUT |
|------|------------------|-----------------------|
| 1    | 0                | IF amplifier selected |
| 1    | 1 <sup>(1)</sup> | Mixer selected        |

- (1) When AISL = 1, RF AGC function is not available at VHF-L band (output level is undefined).

## I<sup>2</sup>C Read Mode ( $R/\overline{W} = 1$ )

**Table 9. Read Data Format**

|                    | MSB |    |   |   |   |    |    | LSB                  |                  |
|--------------------|-----|----|---|---|---|----|----|----------------------|------------------|
| Address byte (ADB) | 1   | 1  | 0 | 0 | 0 | 0  | MA | $R/\overline{W} = 1$ | A <sup>(1)</sup> |
| Status byte (SB)   | POR | FL | 1 | 1 | 1 | A2 | A1 | A0                   | –                |

- (1) A = acknowledge

**Table 10. Read Data Symbol Description**

| SYMBOL | DESCRIPTION                                                                                            | DEFAULT |
|--------|--------------------------------------------------------------------------------------------------------|---------|
| MA     | Address set bit<br>MA = 0 : VLO OSC/AS pin = 0 V (connection to GND)<br>MA = 1 : VLO OSC/AS pin = Open |         |
| POR    | Power-on-reset flag<br>POR set: power on<br>POR reset: end-of-data transmission procedure              | POR = 1 |
| FL     | In-lock flag <sup>(1)</sup><br>FL = 0 : PLL unlocked<br>FL = 1 : PLL locked                            |         |
| A[2:0] | Digital data of ADC (see <a href="#">Table 11</a> )<br>Bit P5 must be set to 0.                        |         |

- (1) Lock detector works by using phase error pulse at the phase detector. Lock flag (FL) is set or reset according to this pulse-width discriminator. Hence, instability of the PLL may cause the lock detection circuit to malfunction. To stabilize the PLL, it is required to evaluate application circuit in various condition of loop-gain (loop filter, CP current) and to verify under operation of the actual application.

**Table 11. ADC Level<sup>(1)</sup>**

| A2 | A1 | A0 | VOLTAGE APPLIED ON ADC INPUT                |
|----|----|----|---------------------------------------------|
| 1  | 0  | 0  | 0.6 V <sub>CC</sub> to V <sub>CC</sub>      |
| 0  | 1  | 1  | 0.45 V <sub>CC</sub> to 0.6 V <sub>CC</sub> |
| 0  | 1  | 0  | 0.3 V <sub>CC</sub> to 0.45 V <sub>CC</sub> |
| 0  | 0  | 1  | 0.15 V <sub>CC</sub> to 0.3 V <sub>CC</sub> |
| 0  | 0  | 0  | 0 V to 0.15 V <sub>CC</sub>                 |

- (1) Accuracy is  $0.03 \times V_{CC}$ .

## Example I<sup>2</sup>C Data Write Sequences

Telegram examples:

Start - ADB - DB1 - DB2 - CB1 – BB - CB2 - Stop

Start - ADB - DB1 - DB2 - Stop

Start - ADB - CB1 - BB - CB2 - Stop

Start - ADB - CB1 - BB - Stop

Start - ADB - CB2 - Stop

Abbreviations:

ADB: Address byte

BB: Band switch byte

CB1: Control byte 1

CB2: Control byte 2

DB1: Divider byte 1

DB2: Divider byte 2

Start: Start condition

Stop: Stop condition

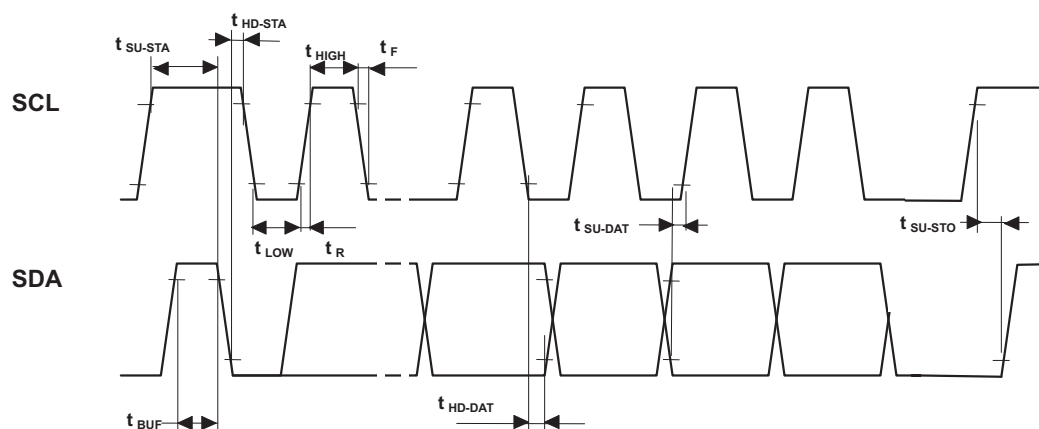
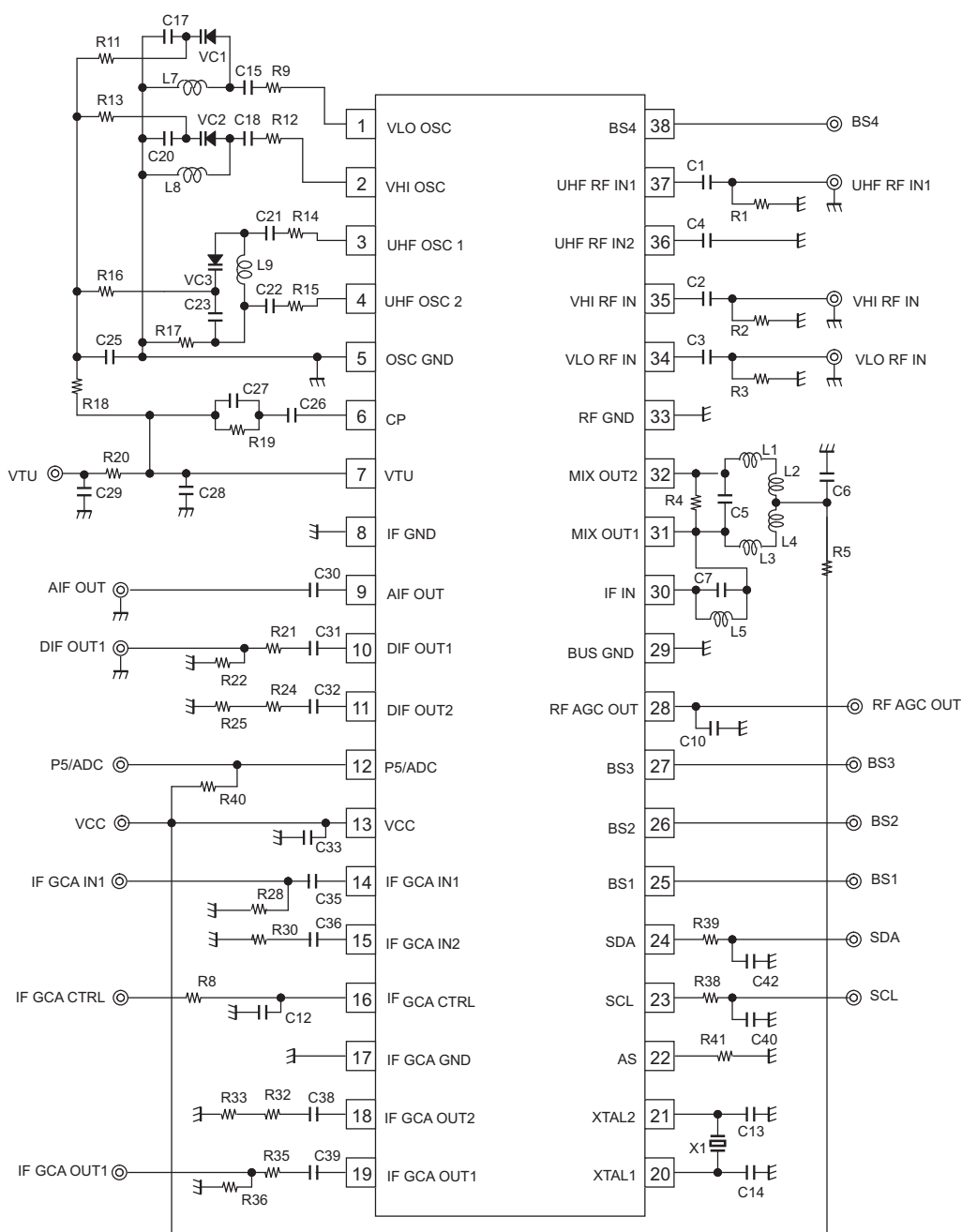


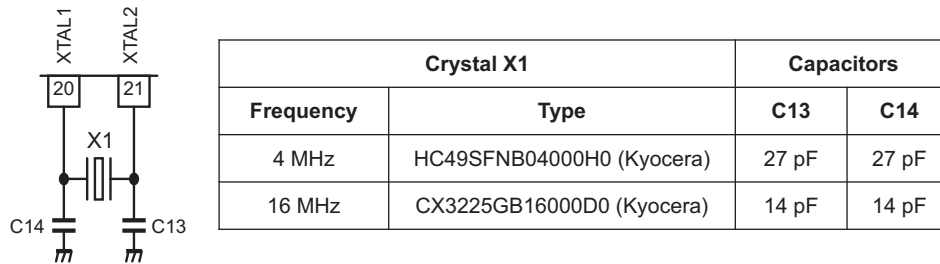
**Figure 23. I<sup>2</sup>C Timing**

## APPLICATION INFORMATION



NOTE: This application information is advisory and performance-check is required at actual application circuits. TI assumes no responsibility for the consequences of use of this circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

**Figure 24. Reference Measurement Circuit**


**Figure 25. Reference Crystal Oscillation Circuit**
**Table 12. Component Values for Measurement Circuit**

| PART NAME         | VALUE     | PART NAME         | VALUE        |
|-------------------|-----------|-------------------|--------------|
| C1 (UHF RFIN1)    | 2.2nF     | R1 (UHF RFIN1)    | Open (51Ω)   |
| C2 (VHI RFIN)     | 2.2nF     | R2 (VHI RFIN)     | Open (51Ω)   |
| C3 (VLO RFIN)     | 2.2nF     | R3 (VLO RFIN)     | Open (51Ω)   |
| C4 (UHF RFIN)     | 2.2nF     | R4 (MIXOUT)       | Open         |
| C5 (MIXOUT)       | 5.5pF     | R5 (MIXOUT)       | 0Ω           |
| C6 (MIXOUT)       | 2.2nF     | R8 (IF GCA CTRL)  | 0Ω           |
| C7 (IF IN)        | 0Ω        | R9 (VLO OSC)      | 0Ω           |
| C10 (RF AGC OUT)  | 0.15μF    | R11 (VLO OSC)     | 3.3kΩ        |
| C12 (IF GCA CTRL) | 0.1μF     | R12 (VHI OSC)     | 10Ω          |
| C13 (XTAL2)       | 27pF      | R13 (VHI OSC)     | 3.3kΩ        |
| C14 (XTAL1)       | 27pF      | R14 (UHF OSC)     | 4.7Ω         |
| C15 (VLO OSC)     | 4pF       | R15 (UHF OSC)     | 4.7Ω         |
| C17 (VLO OSC)     | 68pF      | R16 (UHF OSC)     | 1kΩ          |
| C18 (VHI OSC)     | 10pF      | R17 (UHF OSC)     | 2.2kΩ        |
| C20 (VHI OSC)     | 130pF     | R18 (VTU)         | 3.3kΩ        |
| C21 (UHF OSC)     | 6pF       | R19 (CP)          | 82kΩ         |
| C22 (UHF OSC)     | 6pF       | R20 (VTU)         | 22kΩ         |
| C23 (UHF OSC)     | 20pF      | R21 (DIF OUT1)    | 200Ω         |
| C25 (VTU)         | 2.2nF/50V | R22 (DIF OUT1)    | Open         |
| C26 (CP)          | 3.9nF/50V | R24 (DIF OUT2)    | 200Ω         |
| C27 (CP)          | 10pF/50V  | R25 (DIF OUT2)    | 51Ω          |
| C28 (VTU)         | 150pF/50V | R28 (IF GCA IN1)  | (51Ω)        |
| C29 (VTU)         | 2.2nF/50V | R30 (IF GCA IN2)  | (0Ω)         |
| C30 (AIF OUT)     | 2.2nF     | R32 (IF GCA OUT2) | 200Ω         |
| C31 (DIF OUT1)    | 2.2nF     | R33 (IF GCA OUT2) | 51Ω          |
| C32 (DIF OUT2)    | 2.2nF     | R35 (IF GCA OUT1) | 200Ω         |
| C33 (VCC)         | 0.1μF     | R36 (IF GCA OUT1) | Open         |
| C35 (IF GCA IN1)  | 2.2nF     | R38 (SCL)         | 330Ω         |
| C36 (IF GCA IN2)  | 2.2nF     | R39 (SDA)         | 330Ω         |
| C38 (IF GCA OUT2) | 2.2nF     | R40 (P5)          | Open         |
| C39 (IF GCA OUT1) | 2.2nF     | R41 (AS)          | Open         |
| C40 (SCL)         | Open      |                   |              |
| C42 (SDA)         | Open      | VC1 (VLO OSC)     | KDV270E      |
|                   |           | VC2 (VHI OSC)     | KDV270E      |
|                   |           | VC3 (UHF OSC)     | KDV216E      |
|                   |           | X1                | 4MHz crystal |

**Table 12. Component Values for Measurement Circuit (continued)**

| PART NAME    | VALUE                           | PART NAME | VALUE |
|--------------|---------------------------------|-----------|-------|
| L1 (MIXOUT)  | 470nH (LK1608R47KT Taiyo Yuden) |           |       |
| L2 (MIXOUT)  | 560nH (LK1608R56KT Taiyo Yuden) |           |       |
| L3 (MIXOUT)  | 470nH (LK1608R47KT Taiyo Yuden) |           |       |
| L4 (MIXOUT)  | 560nH (LK1608R56KT Taiyo Yuden) |           |       |
| L5 (IFIN)    | Open                            |           |       |
| L7 (VLO OSC) | φ3.0mm, 9T, wire0.32mm          |           |       |
| L8 (VHI OSC) | φ1.8mm, 4T, wire0.4mm           |           |       |
| L9 (UHF OSC) | φ1.8mm, 2T, wire0.4mm           |           |       |

IF frequency: 36 MHz  
 Local frequency range: VHF-LOW: 87 to 186 MHz  
 VHF-HIGH: 193 to 462 MHz  
 UHF: 470 to 894 MHz

## Test Circuits

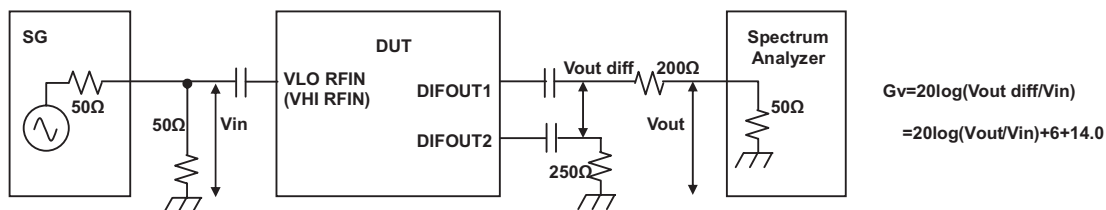


Figure 26. VHF Conversion Gain Measurement Circuit (at DIFOUT)

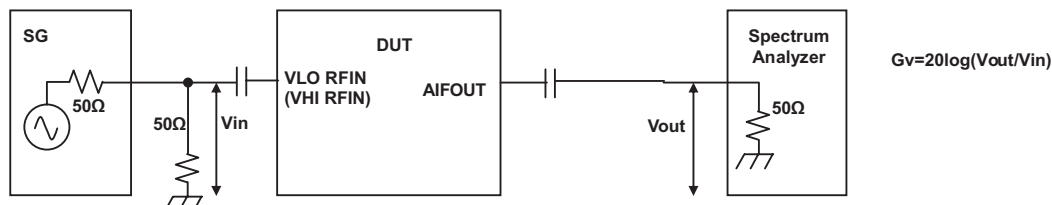


Figure 27. VHF Conversion Gain Measurement Circuit (at AIFOUT)

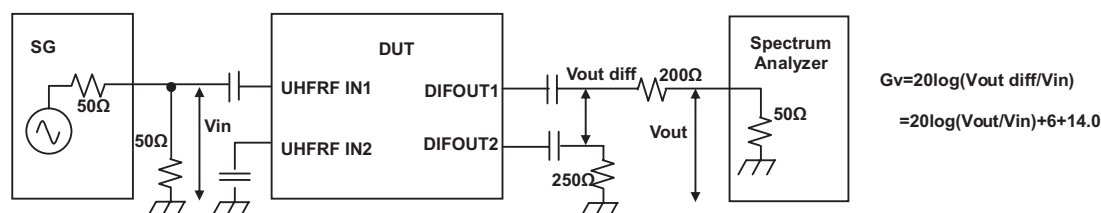


Figure 28. UHF Conversion Gain Measurement Circuit (at DIFOUT)

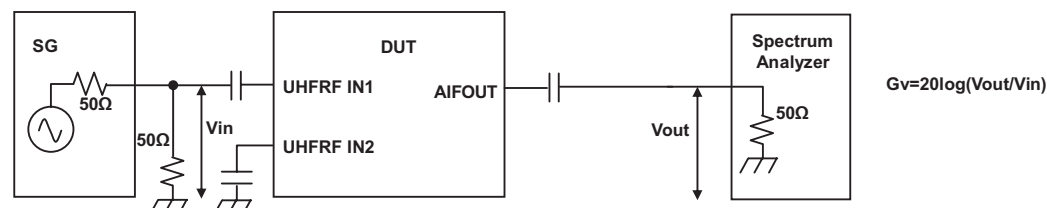


Figure 29. UHF Conversion Gain Measurement Circuit (at AIFOUT)

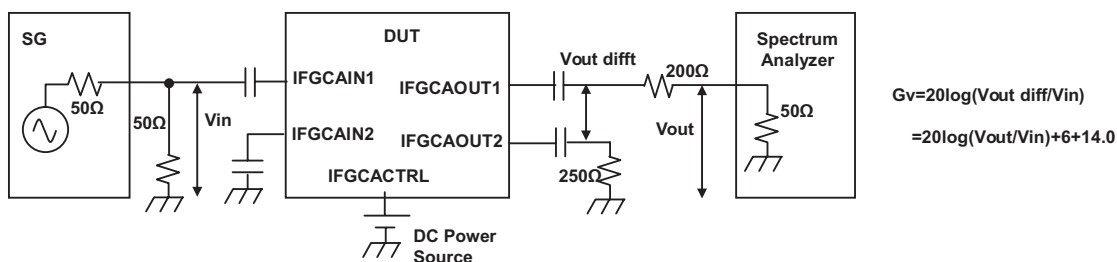
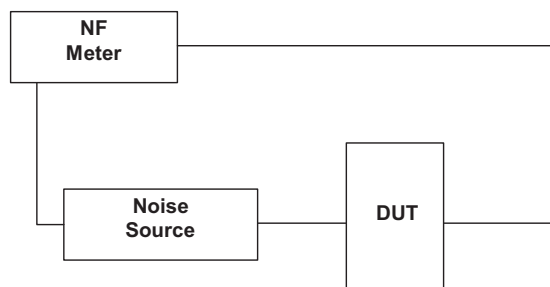
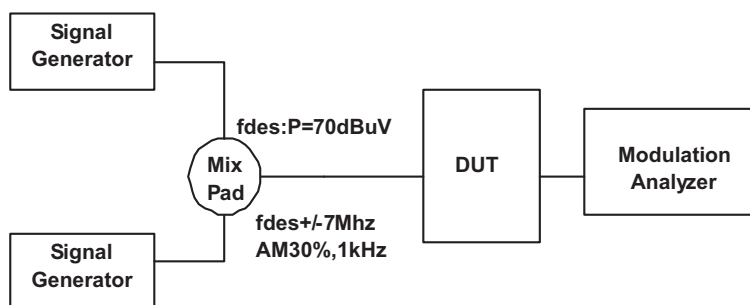


Figure 30. IF GCA Gain Measurement Circuit

**Figure 31. Noise Figure Measurement Circuit****Figure 32. 1% Cross Modulation Distortion Measurement Circuit**

## TYPICAL CHARACTERISTICS

### Band Switch Driver Output Voltage (BS1-BS4)

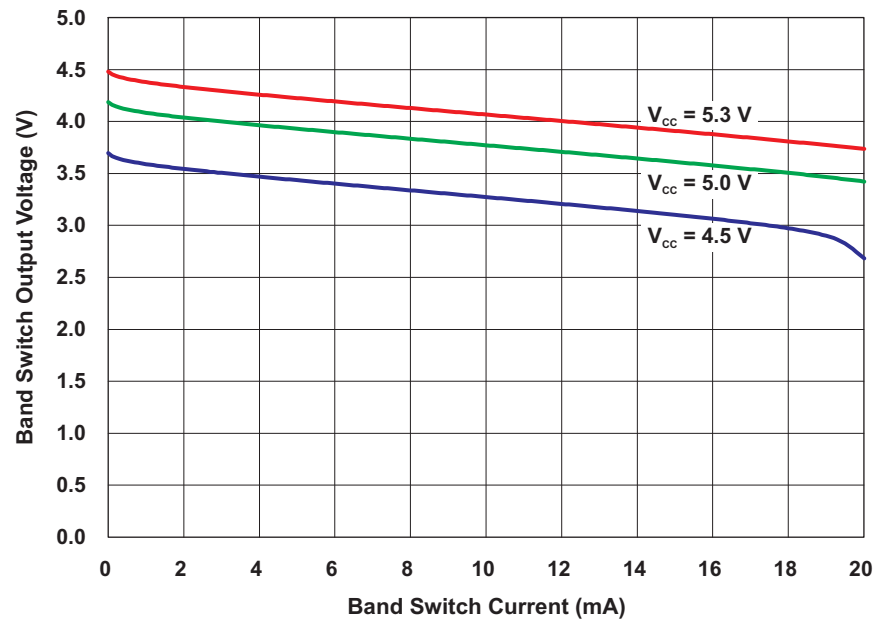


Figure 33. Band Switch Driver Output Voltage

### S-Parameter

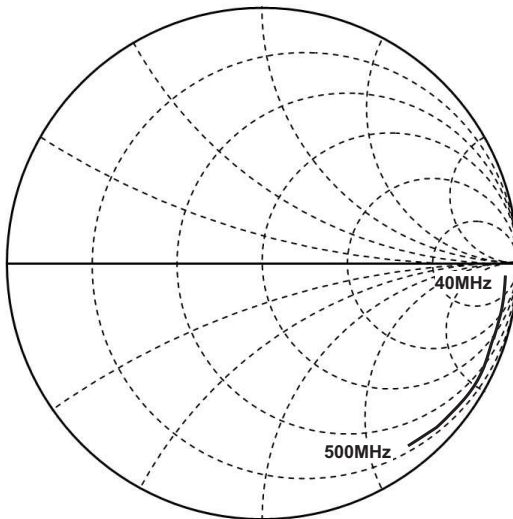


Figure 34. VLO, VHI RFIN

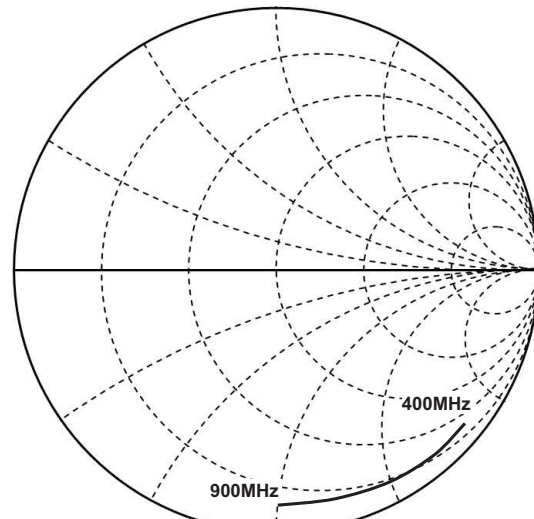


Figure 35. UHF RFIN

## TYPICAL CHARACTERISTICS (continued)

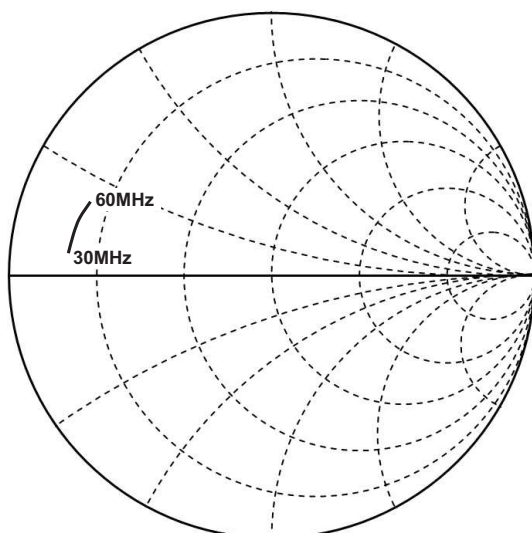


Figure 36. DIFOUT

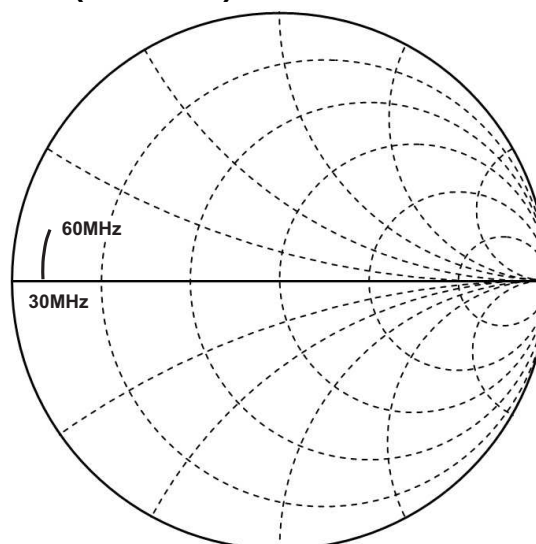


Figure 37. AIFOUT

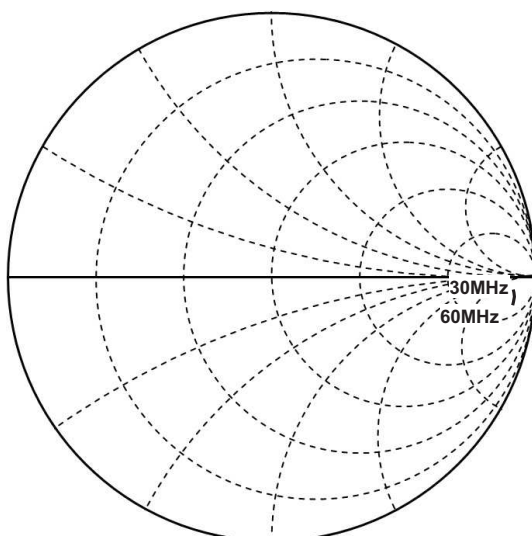


Figure 38. IF GCA IN

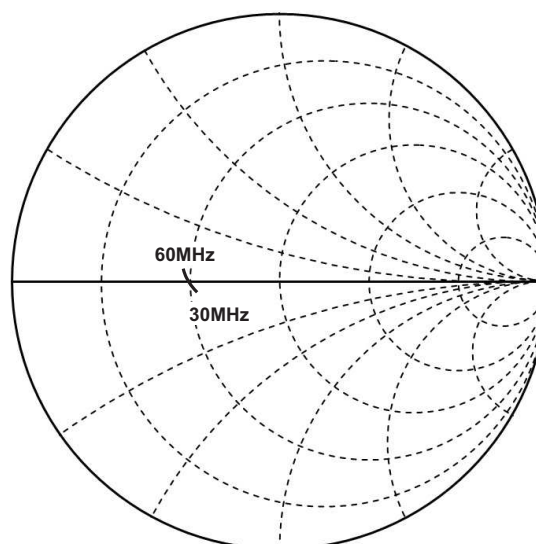


Figure 39. IF GCAOUT

## TYPICAL CHARACTERISTICS (continued)

### IF GCA Gain vs Control Voltage

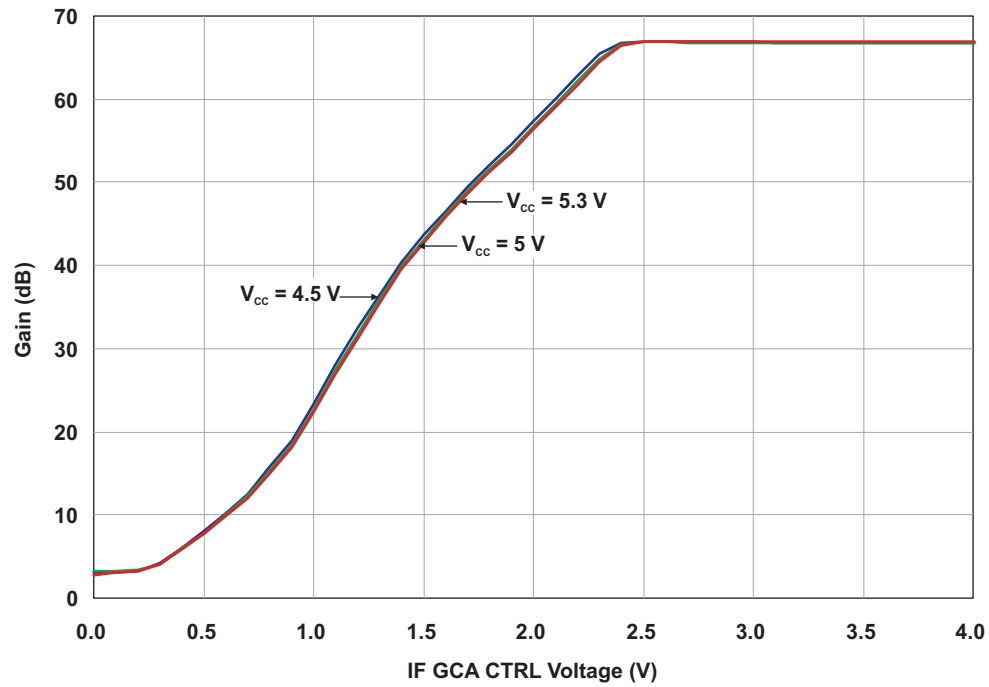


**Figure 40. IF GCA Gain vs Control Voltage**

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|------------------|----------------------|--------------|-------------------------|---------|
| SN761645DBTR     | OBSOLETE      | TSSOP        | DBT                | 38   |                | TBD             | Call TI          | Call TI              | -20 to 85    | B1645                   |         |

(1) The marketing status values are defined as follows:

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**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

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**OBSOLETE:** TI has discontinued the production of the device.

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

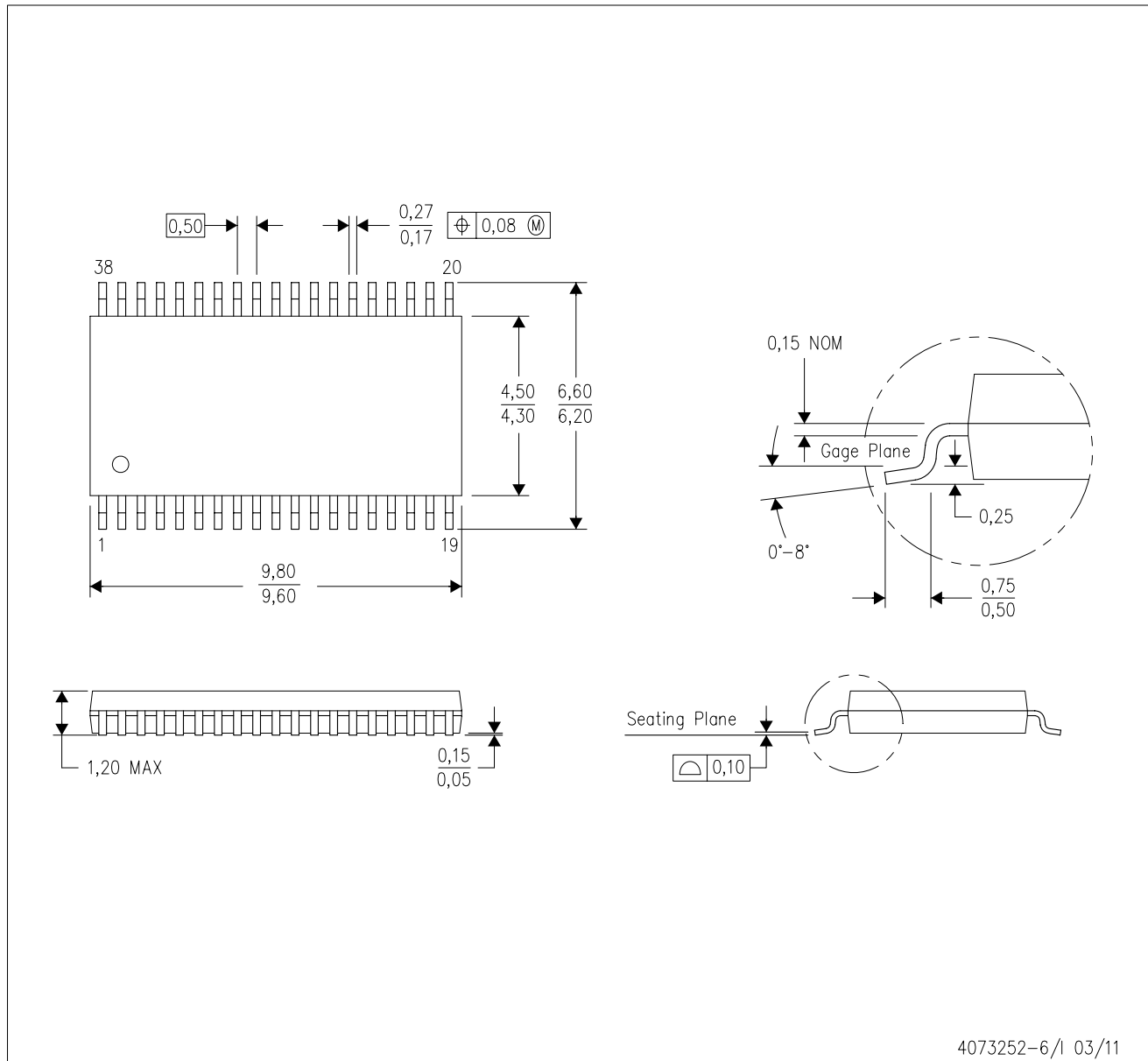
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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DBT (R-PDSO-G38)

PLASTIC SMALL OUTLINE



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  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-153.

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